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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,576	03/22/2004	Robert Tod Dimpsey	AUS920040061US1	2219

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EXAMINER	
WALTER, CRAIG E	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 10/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,576	DIMPSEY ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 13-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 13-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 8/29/06, 5/31/06, 4/25/06, 6/30/05, 10/5/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-9 and 13-24 are pending in the Application.

Claims 1, 2, 13, 14, 22, and 23 have been amended.

Claims 10-12 have been canceled.

Claims 1-9 and 13-24 are rejected.

Information Disclosure Statement

2. The four information disclosure statements submitted on 5 October 2006, 29 August 2006, 31 May 2006, and 25 April 2006 were fully considered by the Examiner.

3. The information disclosure statement filed 4 August 2006 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because all three pages are completely blank. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

4. Line item BM (as listed on page 2 of the Information Disclosure Statement filed on 30 June 2006) was considered. The previous Examiner did not consider this reference upon issuing the previous Office action (previous Examiner asserted that no

English translation of the abstract is present), however current Examiner agrees that the translation was available to the Examiner upon filing of the IDS. Line item BJ as listed on this very page however was not considered, as the English translation of the abstract is not present (see the discussion under the heading Response To Arguments, *infra*). Current Examiner did not consider the remaining items on the IDS at this time, as the previous Examiner has already considered these references at the time the previous Office action was issued.

Response to Amendment

5. Applicant's amendments and arguments filed on 4 August 2006 in response to the office action mailed on 4 May 2006 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 5-15, 17-24 rejected under 35 U.S.C. 102(b) as being anticipated by Hervin et al. (US Patent 5,805,879), hereinafter Hervin.

With respect to claim 1, Hervin discloses a method in a data processing system for generating coverage data for accesses to data during execution of code in the data processing system, the method comprising:

Detecting that access to data in a memory location having a data access indicator associated therewith has occurred during execution of an instruction in the code at a processor in the data processing system; and [(processor determines if the access indicator is to be set) column 3, lines 37-39]. See also col. 12, line 60 through col. 13, line 33.

changing a state of the data access indicator by the processor when the instruction is executed, for generating coverage data for accesses to data during execution of the code by the processor. [(whenever a memory is first accessed, set the access indicator associated therewith) column 3, lines 27-29]. See also col. 12, line 60 through col. 13, line 33.

Further supplementing these assertions, Hervin's teachings can be interrupted to anticipate claim 1 in at least two unique ways. First, Fig. 7 describes Hervin's exception handling routine (i.e. instruction), which occurs between steps 715 and 740. The data access indicator in changed when the exception handling is executed upon determining that the access bit is not set (i.e. step 730). Also note access to the data in memory is in fact detected during the execution of step 715. More specifically, the determining step set forth in step 715 is used to determine if the memory has been accessed in general (including if access occurs during the execution of the exception instruction or not) – col. 12, line 60 through col. 13, line 33. In other words, if the access occurs

during execution of the instruction, the access bit will reflect this access based on its setting, as the access bit is used to determine if the memory location has been accessed, and the bit is changed if and only if the system determines that it needs to be set when the exception handling instruction is executed. The exception handling instruction terminates upon reaching step 740 in which normal processing resumes.

Secondly, the instruction as recited in line 4 of claim 1 can be construed as any instruction executed by the processor. Hervin's processor is in fact pipelined, indicating that detecting the access of the memory location (which is indicated by the access indicator) occurs during the execution of said instruction, rather upon completion. As described above, Hervin teaches changing the state of the indicator (a point that Applicant concedes), however the question is if the changing occurs "when the instruction is executed". Examiner's broadest reasonable interruption of the claim consistent with Applicant's specification does not in fact limit "when" to mean "simultaneous". When in fact may be broadly be interrupted as "upon", or "on or after". Since Hervin's indicator will not be changed until the memory is accessed, it must only be changed "when" the execution of access occurs, otherwise the bit would have never changed.

With respect to claim 2, Hervin discloses the method of claim 1, wherein the changing step comprises:

receiving a signal at a data cache in the processor generated by a completion buffer in the processor indicating that data in the memory location has been accessed during the execution of the instruction; and [(segment descriptor is retrieved from memory)

column 4, lines 24-43]. Also note the processor comprising the buffer generates the indicator status.

responsive to receiving the signal, changing the state of the access indicator by the data cache. [(when memory is accessed, the access indicator bit is changed) column 4, lines 24-43]

With respect to claim 3, Hervin discloses the method of claim 1, wherein the access indicator is located in a field in the instruction. [(instructions load segment access indicator) column 4, lines 14-24]

With respect to claim 5, Hervin discloses the method of claim 1, wherein the access indicator associated with the instruction is located in a page table. [(page tables in memory) column 8, line 52]

With respect to claim 6, Hervin discloses the method of claim 1, wherein the memory location accessed during the execution of the code have set data access indicators when the state of the access indicators associated with the executed instruction are changed, while the memory location un-accessed during the execution of the code have unset data access indicators because the state of the unset data access indicators remain unchanged. [(changing the memory access indicator only associated with the memory that is accessed) column 3, lines 27-29]

With respect to claim 7, Hervin discloses the method of claim 1, wherein data access indicators are associated with every memory location within the code. [(segment descriptor containing access indicator is associated with every segment of memory) column 10, lines 53-64]

With respect to claim 8, Hervin discloses the method of claim 1, wherein data access indicators are associated only with selected memory locations. [(to set access indicator associated with memory access by processor) column 13, lines 37-40]

With respect to claim 9, Hervin discloses the method of claim 1, wherein the memory location is at least one of a byte, (column 11, line 4) a word, (column 9, line 55) and a double word. (column 9, line 57)

Claims 10, 11 and 12 rejected with same rationale as claims 1 and 2.

Claims 13 and 22 rejected with same rationale as claim 1.

Claims 14 and 23 rejected with same rationale as claim 2.

Claim 15 rejected with same rationale as claim 3.

Claim 17 rejected with same rationale as claim 5.

Claims 18 and 24 rejected with same rationale as claim 6.

Claim 19 rejected with same rationale as claim 7.

Claim 20 rejected with same rationale as claim 8.

Claim 21 rejected with same rationale as claim 9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4 and 16 rejected under 35 U.S.C 103 (a) as being unpatentable over Hervin (US Patent 5,805,879) as applied to claims 1 and 13 above, and in view of Sederlund et al. (US Patent 6,647,301), hereinafter Sederlund.

As per claim 4, Hervin does not disclose expressly the method of claim 1, wherein the access indicator associated with the instruction is located in a shadow memory. However, Sederlund discloses using a memory access error indicator with shadow memory. (column 38, lines 1-5)

Hervin et al and Sederlund are analogous art because they are from same field of endeavor, namely memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the shadow memory of Sederlund into the system of Hervin. The motivation for doing so would have been to increase the versatility of the system of Hervin.

Claim 16 rejected with same rationale as claim 4.

Response to Arguments

8. Applicant's amendments and arguments filed on 4 August 2006 in response to the office action mailed on 4 May 2006 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

9. Response to arguments under heading II. Information Disclosure Statement:

Applicant's assertion that the article labeled BM on page 2 of the Information Disclosure Statement filed June 30, 2005 contained an English

translation of the abstract as originally filed is persuasive, and as such, the item has been fully considered by the current Examiner. Applicant's assertion that the article labeled BJ on page 2 of the Information Disclosure Statement filed June 30, 2005 contained an English translation of the abstract as originally filed is not persuasive. Current Examiner cannot locate an English translation of the abstract for this item during original filing, therefore this item has not been considered by the Examiner.

10. Response to arguments under heading III. 35 U.S.C. § 102, Anticipation:

As for claim 1, Applicant asserts that "Hervin does not teach or suggest "detecting that access to data in a memory location having a data access indicator associated therewith has occurred during execution of an instruction in the code at a processor in the data processing system"; or "changing a state of the data access indicator by the processor when the instruction is executed for generating coverage data for accesses to data during execution of the code by the processor"". Applicant further concedes that Hervin in fact teaches setting a segment access indicator associated with a segment of system memory being accessed by a processor, however alleges that Hervin's disclosure operates differently than in the present invention as recited in amended claim 1. Applicant refers to a superset of lines cited by the previous Examiner as evidence that Hervin teaches setting an access indicator after (emphasis added) the execution processing stage of the processor rather than "during execution of an instruction in the code at a processor in the data processing system". This argument

however is not persuasive. More specifically, regardless of the teaching contained within Hervin's *background*, he still does in fact teach "detecting that access" during the execution and "changing a state of a data indicator" when the instruction is executed as required by the limitations recited in this claim.

Examiner asserts that, by giving the base claims their broadest reasonable interpretation consistent with the specification (see MPEP § 2111), Hervin's teachings can be interrupted to anticipate claim 1 in at least two unique ways. First, Fig. 7 describes Hervin's exception handling routine (i.e. instruction), which occurs between steps 715 and 740. The data access indicator in changed when the exception handling is executed upon determining that the access bit is not set (i.e. step 730). Also note access to the data in memory is in fact detected during the execution of step 715. More specifically, the determining step set forth in step 715 is used to determine if the memory has been accessed in general (including if access occurs during the execution of the exception instruction or not) – col. 12, line 60 through col. 13, line 33. In other words, if the access occurs during execution of the instruction, the access bit will reflect this access based on its setting, as the access bit is used to determine if the memory location has been accessed, and the bit is changed if and only if the system determines that it needs to be set when the exception handling instruction is executed. The exception handling instruction terminates upon reaching step 740 in which normal processing resumes.

Secondly, the instruction as recited in line 4 of claim 1 can be construed as any instruction executed by the processor. Hervin's processor is in fact pipelined, indicating that detecting the access of the memory location (which is indicated by the access indicator) occurs during the execution of said instruction, rather upon completion. As described above, Hervin teaches changing the state of the indicator (a point that Applicant concedes), however the question is if the changing occurs "when the instruction is executed". Examiner's broadest reasonable interruption of the claim consistent with Applicant's specification does not in fact limit "when" to mean "simultaneous". When in fact may be broadly be interrupted as "upon", or "on or after". Since Hervin's indicator will not be changed until the memory is accessed, it must only be changed "when" the execution of access occurs, otherwise the bit would have never changed.

Similar reasoning applies to Applicant's assertion in claim 2 that Hervin fails to teach, "that the state of the segment access descriptor is changed "in response to receiving a signal generated by a completion buffer in the processor indicating that data in the memory location has been accessed during the execution of the instruction"". With respect to the first interruption, Hervin's access bit notifies if the system if the memory has been accessed in general, including during the execution of exception handling. With respect to the second interpretation, the access must occur during the execution (as per the discussion *supra*), hence if when the indicator is indicating that the memory has been

accessed, the system knows it has been accessed when the instruction to do so executed.

11. Response to arguments under heading IV. 35 U.S.C. § 103, Obviousness:

Applicant's argument that Sederlund fails to supply the deficiencies of Hervin's disclosure is rendered moot as Examiner maintains that Hervin in fact teaches all of the claimed limitations of the amended base claims per the rejections and arguments presented *supra*.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

13. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

10/15/06

MANO PADMANABHAN
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